L14: Entry 1 of 3 File: USPT Jun 7, 2005

DOCUMENT-IDENTIFIER: US 6903571 B1
TITLE: Programmable systems and devices with multiplexer circuits providing enhanced capabilities for triple modular redundancy

Abstract Text (1):
Programmable systems and devices that include programmable multiplexers designed to minimize the impact of single event upsets (SEUs) on triple modular redundancy (TMR) circuits. In a programmable routing multiplexer, each path through the multiplexer is controlled by a different configuration memory cell. A unidirectional buffer is included on each routing path through the multiplexer. Therefore, an SEU changing the state of any single memory cell does not short together any two input terminals of the multiplexer. Hence, when a TMR circuit is implemented using the multiplexer, an SEU affecting the multiplexer causes no more than one TMR module to become defective. The other two TMR modules together provide the correct output signal, outvoting the defective module, and the circuit continues to operate correctly.

Brief Summary Text (7):
When subjected to unusual conditions such as cosmic rays or bombardment by neutrons or alpha particles, a static memory cell can change state. For example, a stored high value can be inadvertently changed to a low value, and vice versa. Sometimes these "single event upsets" (SEUs) have no effect on the functionality of the chip, for example, when the static memory cell controls a pass gate between two unused interconnect lines. At other times, an SEU can change the functionality of a configured PLD such that the circuit no longer functions properly.

Brief Summary Text (8):
FIG. 2 shows an exemplary programmable routing multiplexer circuit in a PLD. This type of circuit is commonly included in FPGA interconnect structures, for example. The number of input signals varies and is often greater than eight, but eight input signals are shown in the exemplary circuits herein, for clarity. The circuit selects one of several different input signals and passes the selected signal to an output node. As will be explained, an SEU affecting one of the configuration memory cells in the circuit can short together two of the multiplexer input terminals.

Brief Summary Text (12):
In the multiplexer circuit of FIG. 2, the upset of any single memory cell (i.e., any SEU affecting any of memory cells M0-M7) causes a failure in the circuit. For example, assume that memory cell M0 stores a high value, while memory cells M1-M7 store low values. Pass gate 200 is enabled, and the selected input signal is IN0. Pass gates 201-207 are disabled. If the value in memory cell M0 is upset (i.e., changes to a low value), the path from input terminal IN0 to output terminal OUT is broken, and output signal OUT is no longer actively driven by node IN0. If the value in-memory cell M4 is upset (i.e., changes to a high value), pass gate 204 is enabled and there is a "short" (an inadvertent coupling) between input terminals IN0 and IN4. Similarly, if the value in memory cell M5 is upset, pass gate 205 is enabled and there is a short between nodes IN0 and IN5, and so forth. Thus, an SEU affecting one of the configuration memory cells in the circuit of FIG. 2 can short together two of the multiplexer input terminals.

Brief Summary Text (13):
Further, as operating voltages diminish, static memory cells become more susceptible to changes in state caused by SEUs. To reduce manufacturing costs, PLD manufacturers are aggressively reducing device sizes in their. PLDs. These smaller devices often operate at lower voltages. Therefore, all else being equal, there is a tendency towards greater SEU susceptibility in PLDs.

Brief Summary Text (14):
Circuits and methods have been developed to avoid the problems associated with SEUs. One well-known strategy for avoiding such problems is illustrated in FIG. 3. The illustrated circuit is called a triple modular redundancy (TMR) circuit. In essence, the required logic is implemented three times (i.e., in three modules), and the results generated by the three modules are compared. Any two module output signals that are the same are considered to be correct, and if the third module provides a different result the "dissenting vote" is thrown out.

Brief Summary Text (16):
Clearly, this approach overcomes any SEU that affects the functionality of only one of the three modules M1-M3. The module affected by the event produces an incorrect result, which is overridden in the voting circuit by the other two modules. However, while the circuit of FIG. 3 works well for errors that occur within one of modules M1-M3, it does not work when two of the three modules are in error, causing two of the three inputs to the voting circuit to be incorrect. Such a situation can occur, for example, when an SEU causes a short between two input terminals of a routing multiplexer, and the two input terminals are coupled to nodes in two different modules.

Brief Summary Text (18):
Similarly, SEUs can cause inadvertent connections between a node in one of the modules M1-M3 and a node in the voting circuit VC, or between two different nodes in voting circuit VC, or between nodes in two different voting circuits.

Brief Summary Text (19):
Therefore, it is desirable to facilitate the use of TMR in programmable systems and devices by providing programmable routing multiplexer circuits in which the input terminals cannot be shorted together by a single SEU.

Brief Summary Text (21):
The invention provides programmable systems and devices that include programmable multiplexers designed to minimize the impact of single event upsets (SEUs) on triple modular redundancy (TMR) circuits. In a programmable routing multiplexer, each path through the multiplexer is controlled by a different configuration memory cell. A unidirectional buffer is included on each routing path through the multiplexer. Therefore, an SEU changing the state of any single memory cell does not short together any two input terminals of the multiplexer. Hence, when a TMR circuit is implemented using the multiplexer, an SEU affecting the multiplexer causes no more than one TMR module to become defective. The other two TMR modules together provide the correct output signal, outvoting the defective module, and the circuit continues to operate correctly.

Brief Summary Text (25):
According to another aspect of the invention, a system is controlled by memory cells susceptible to SEUS. The system includes a plurality of logic circuits, a plurality of interconnect lines, and plurality of programmable routing multiplexer circuits programmably interconnecting the interconnect lines with each other and with the logic circuits. Each of the programmable routing multiplexer circuits includes a plurality of multiplexer input terminals, a multiplexer output terminal, a plurality of memory cells susceptible to SEUs, and plurality of unidirectional logic circuits. Each unidirectional logic circuit has an input terminal coupled to an associated multiplexer input terminal, an output terminal coupled to the

multiplexer output terminal, and a control terminal coupled to an output terminal of an associated memory cell.

Detailed Description Text (3):
The invention provides a multiplexer circuit that isolates the input terminals of the multiplexer circuit from each other even in the event of an SEU, by including a unidirectional logic circuit on each path through the multiplexer circuit. FIGS. 4 and 5 illustrate two exemplary implementations.

Detailed Description Text (7):
In some embodiments (i.e., where buffer 410 is implemented in the same fashion as buffer BUF of FIG. 2), the multiplexer circuit of FIG. 4 operates as shown in Table 1. However, in the circuit of FIG. 4, an SEU that affects any of the configuration memory cells M0-M7 cannot cause a short between any of the input terminals IN0-IN7.

Detailed Description Text (8):
When the multiplexer circuit of FIG. 4 is correctly configured, only one of memory cells M0-M7 stores a high value at any given time. For example, suppose memory cell M0 stores a high value and memory cells M1-M7 each store a low value. Pass gate 200 is on (enabled) and pass gates 201-207 are all off (disabled). Input signal IN0 is passed to internal node INT. If the value stored in memory cell M1 flips from low to high due to an SEU, both of input signals IN0 and IN1 are passed to internal node INT, probably resulting in an error at internal node INT and output terminal OUT. However, the voltage level on internal node INT is not passed back to either of input terminals IN0 and IN1, due to the presence of unidirectional buffers 400-401.

Detailed Description Text (9):
For example, suppose a TMR circuit is implemented in a PLD that includes the multiplexer circuit of FIG. 4. Output signal OUT can be included in a TMR module or in the voting circuit. If signal OUT is part of the voting module, an SEU affecting signal OUT will render the TMR circuit inoperable. However, if signal OUT is part of one of the TMR modules, an SEU affecting signal OUT affects only that module. Unlike the multiplexer circuit of FIG. 2, the SEU cannot cause errors in two different TMR modules. Thus, the voting circuit performs its function of disregarding the erroneous signal from the affected module, and the TMR circuit continues to function properly.

Detailed Description Text (11):
FIG. 5 shows another implementation of the invention, in which the unidirectional logic circuits are implemented as tristate buffers. The circuit of FIG. 5 is similar to that of FIG. 4, except that the unidirectional buffers and pass gates are replaced by unidirectional tristate buffers. As in the circuit of FIG. 4, the input terminals cannot be shorted together by a single SEU. The circuit of FIG. 5 includes eight input terminals IN0-IN7, eight unidirectional tristate buffers 500-507, eight configuration memory cells M0-M7, and an output buffer 510.

CLAIMS:

12. A system controlled by memory cells susceptible to single event upsets (SEUs), the system comprising: a plurality of logic circuits; a plurality of interconnect lines; and a plurality of programmable routing multiplexer circuits programmably interconnecting the interconnect lines with each other and with the logic circuits, wherein each of the programmable routing multiplexer circuits comprises: a plurality of multiplexer input terminals; a multiplexer output terminal; a plurality of memory cells susceptible to SEUs; and a plurality of unidirectional logic circuits, each unidirectional logic circuit having an input terminal coupled to an associated multiplexer input terminal, an output terminal coupled to the multiplexer output terminal, and a control terminal coupled to an output terminal

of an associated memory cell.

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L5: Entry 4 of 4 File: USPT Mar 7, 2000

DOCUMENT-IDENTIFIER: US 6034946 A
TITLE: Selection of routing paths in data communications networks to satisfy multiple requirements

Brief Summary Text (7):
Data communications networks may operate via circuit-switching, packet-switching, or a combination of the two. In circuit-switched networks, a private transmission path is created through the network in response to a transmission request. This private path is held for the duration of the communication between the source node and the destination node, and other users are not allowed access to the resources comprising the routing path until after the entire communication has been completed. In packet-switched networks, blocks of data (data packets) are once again transferred from the source node to the destination node along a path in the network, but blocks of data which are part of the same communication need not always use the same path. Moreover, as a particular path in the network is not reserved for any particular communication, network users may share the same resources during the course of a single communication.

Detailed Description Text (74):
As shown in FIG. 3, in a third embodiment of the present invention, it is possible to further increase the probability of identifying a routing path satisfying the dual delay requirements of Equations (2a) and (2b) if the minimum propagation time (p.sub.min) between the source and destination node is known (block 14). In this situation, there is no need to search the region of FIGS. 4-6 where P<p.sub.min to find acceptable paths, as no such paths will be found. Thus, as shown in FIG. 7, line 70 may be redrawn as line 70' so that it extends from the point (0,c.sub.1) to the point where the line P=p.sub.min (line 71) intersects line 67. This latter point has coordinates (x.sub.0, p.sub.min), where:

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Brief Summary Text (21):
The invention provides programmable systems and devices that include programmable multiplexers designed to minimize the impact of single event upsets (SEUs) on triple modular redundancy (TMR) circuits. In a programmable routing multiplexer, each path through the multiplexer is controlled by a different configuration memory cell. A unidirectional buffer is included on each routing path through the multiplexer. Therefore, an SEU changing the state of any single memory cell does not short together any two input terminals of the multiplexer. Hence, when a TMR circuit is implemented using the multiplexer, an SEU affecting the multiplexer causes no more than one TMR module to become defective. The other two TMR modules together provide the correct output signal, outvoting the defective module, and the circuit continues to operate correctly.

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END OF SEARCH HISTORY